

FIG. 1

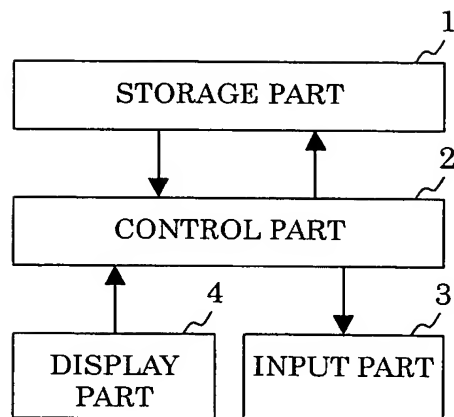


FIG. 2

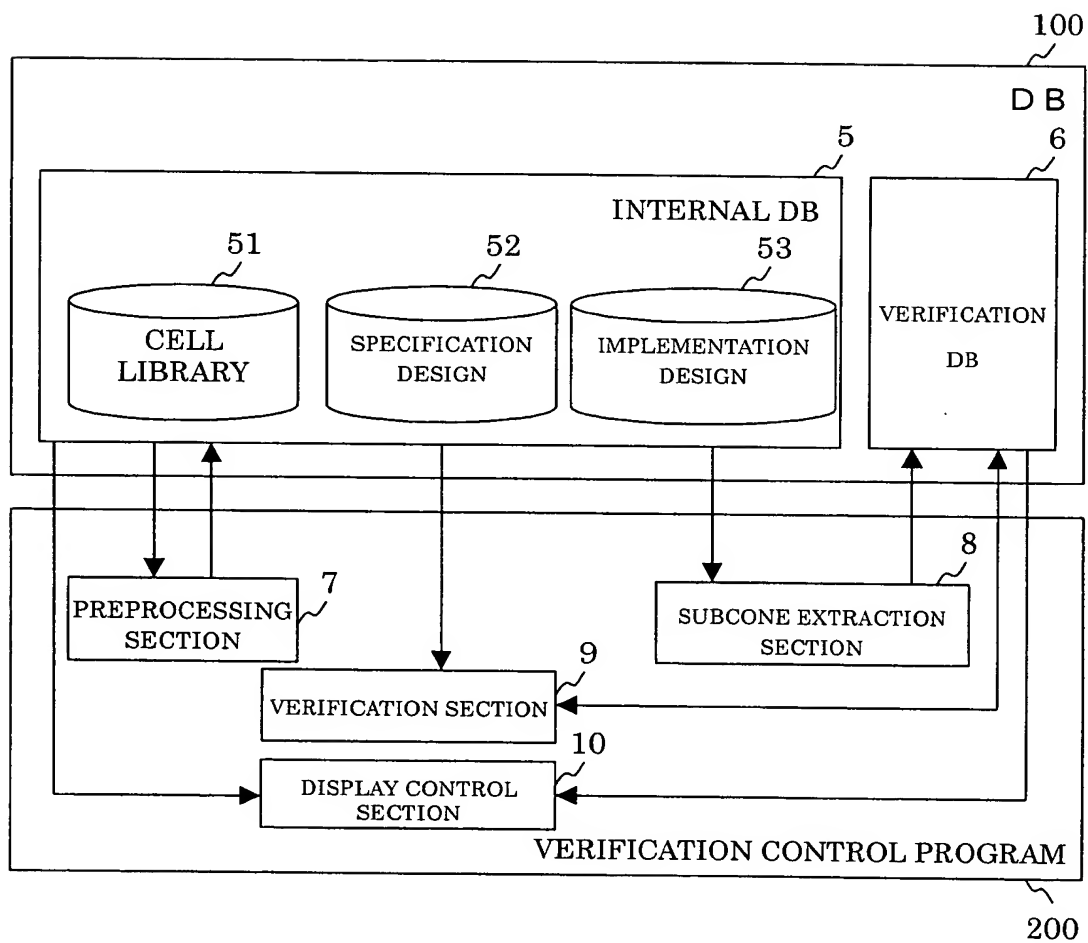


FIG. 3

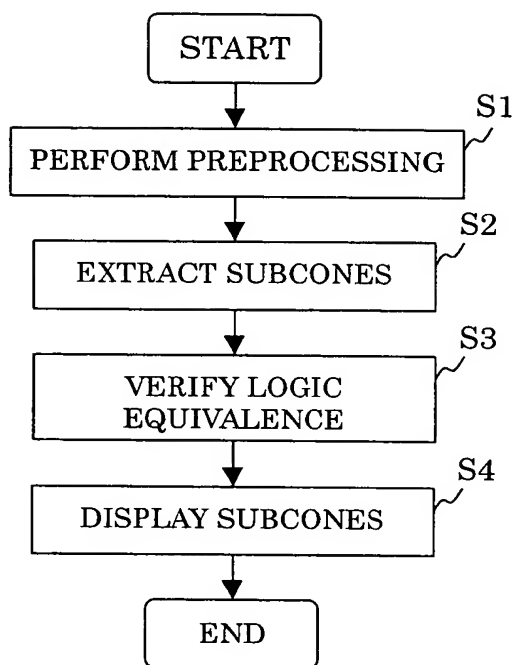


FIG. 4A

FIG. 4B

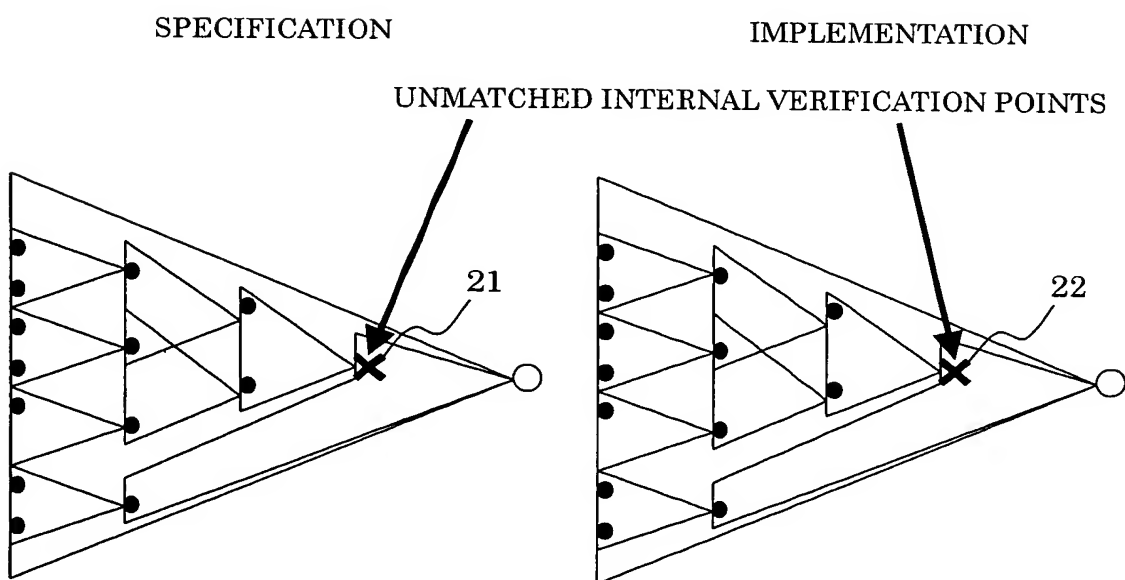


FIG. 5

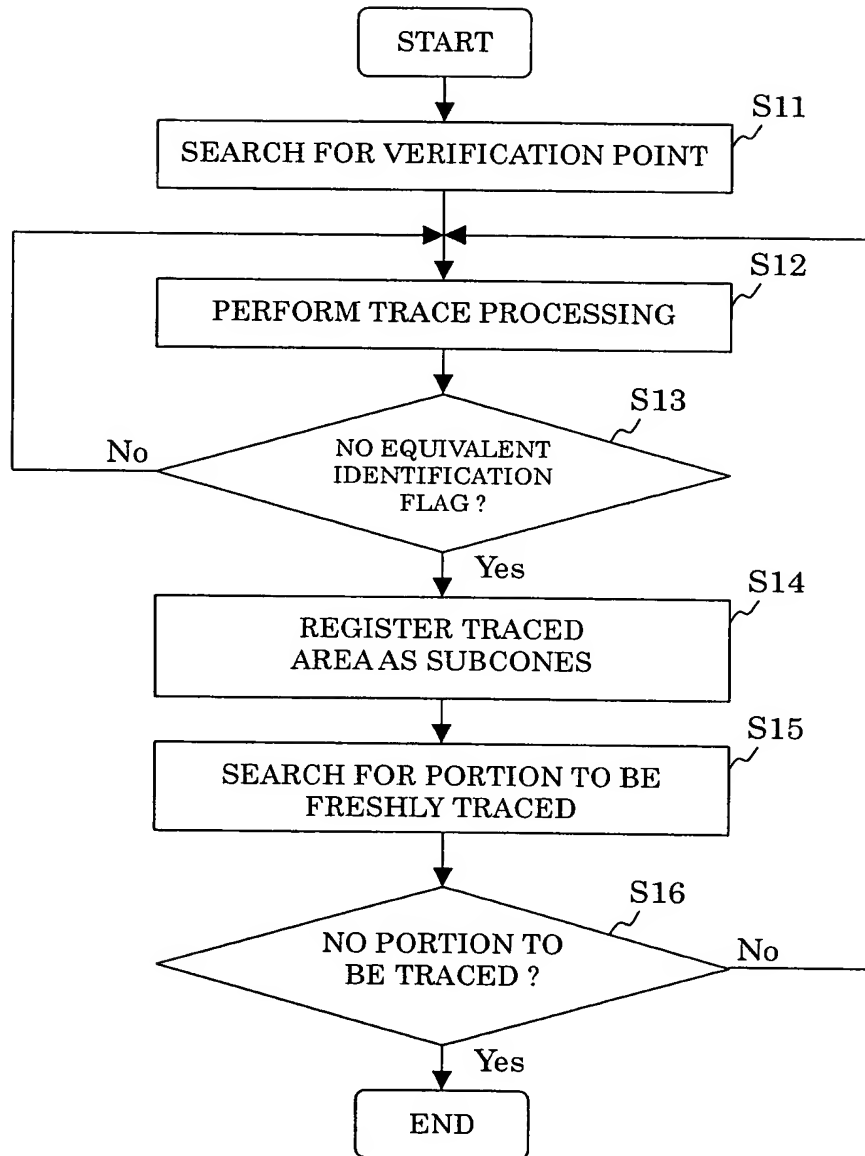


FIG. 6A

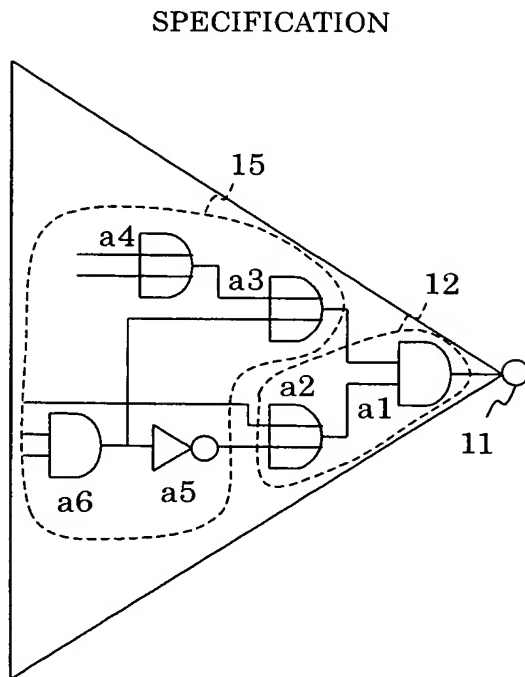


FIG. 6B

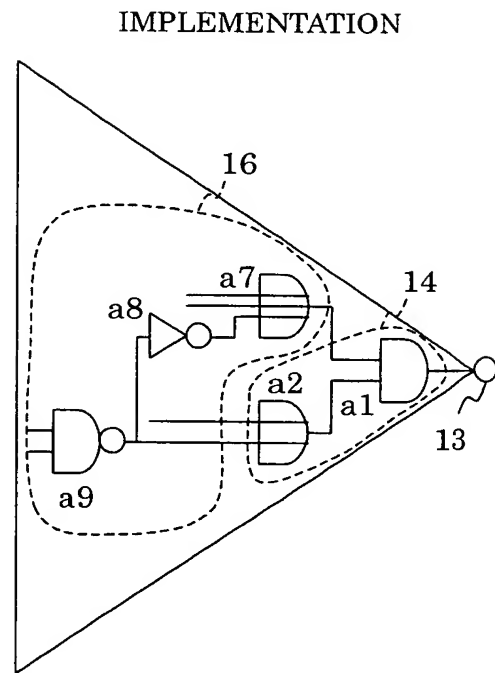


FIG. 7A

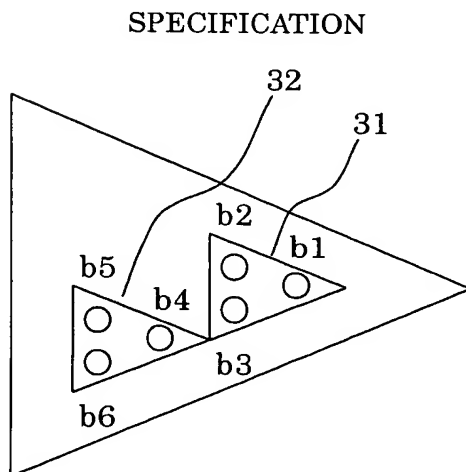


FIG. 7B

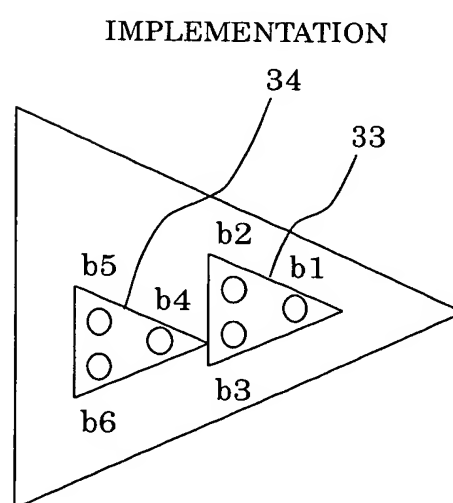


FIG. 8

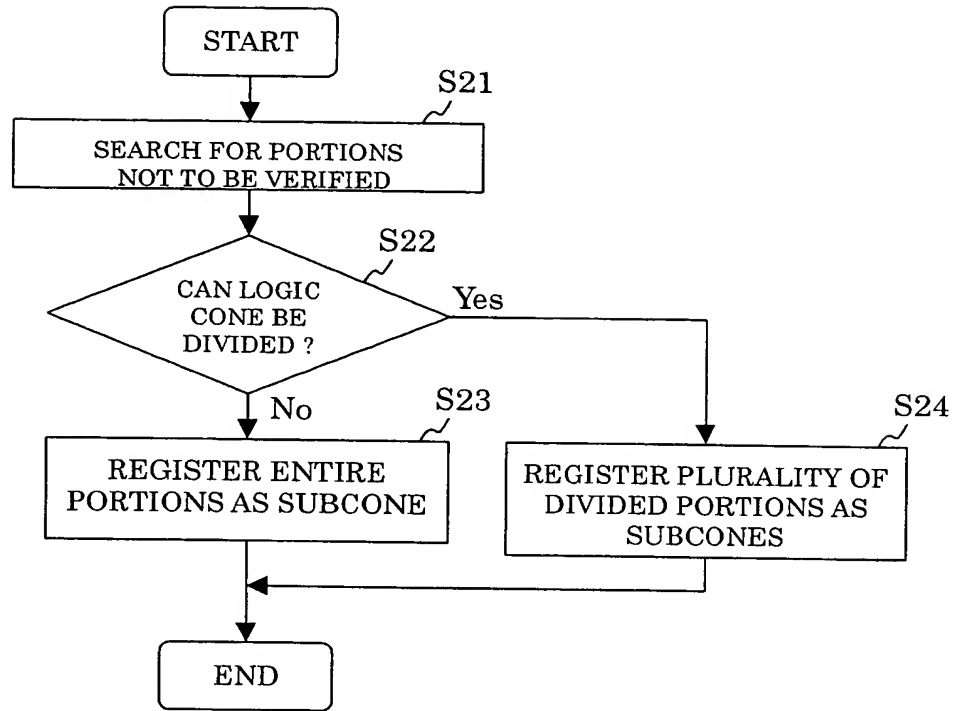


FIG. 9A

SPECIFICATION

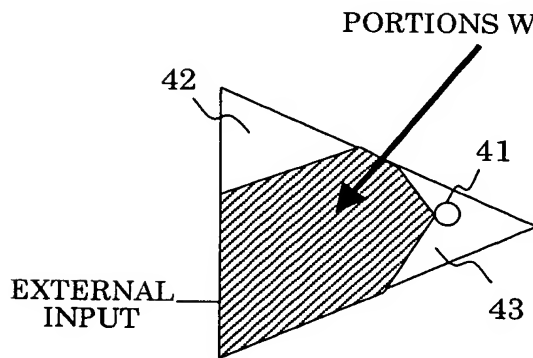


FIG. 9B

IMPLEMENTATION

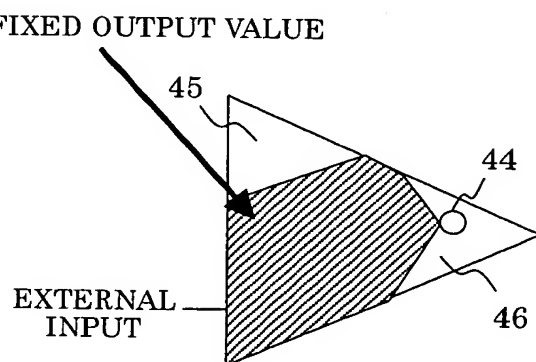


FIG. 10

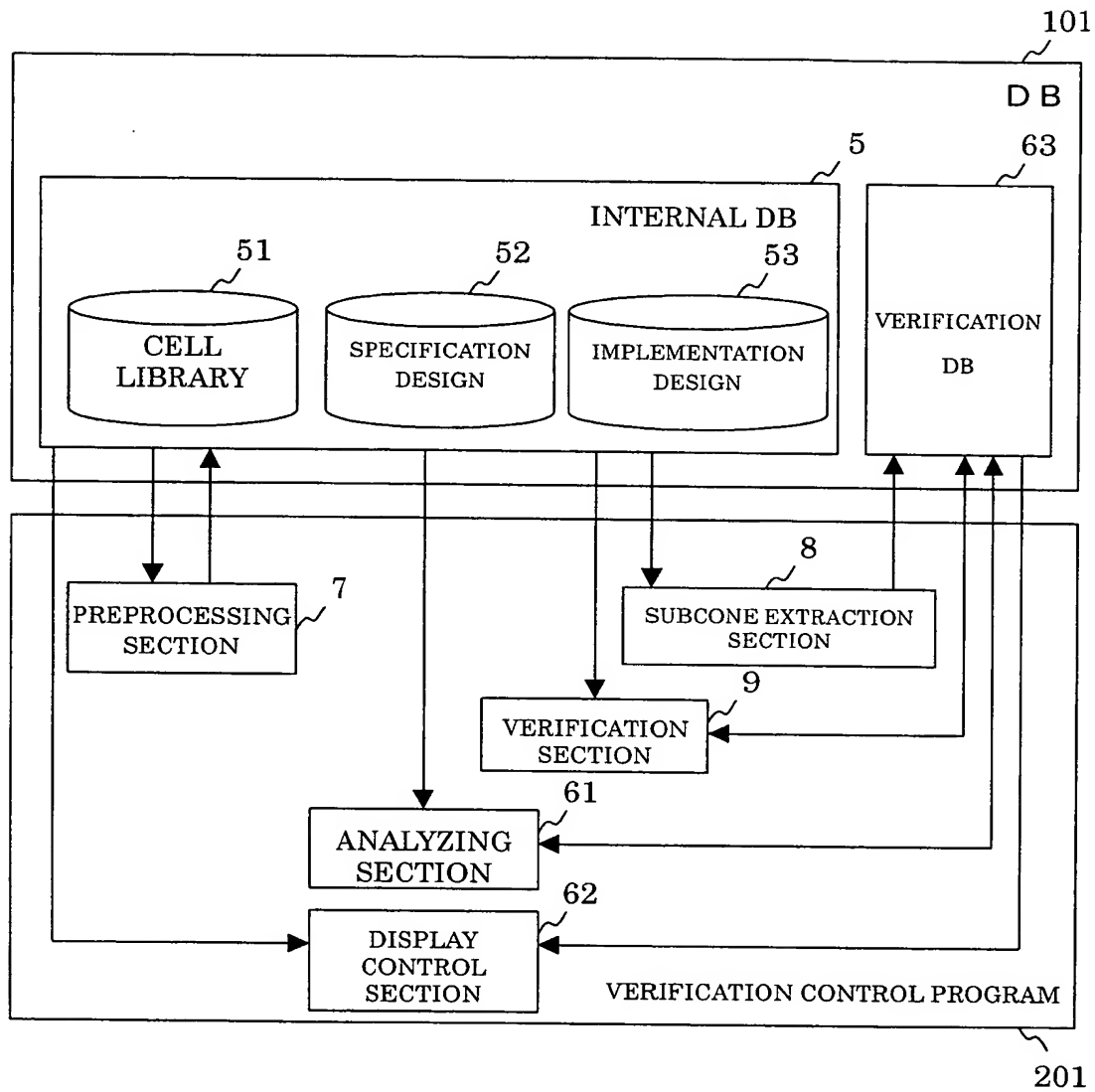


FIG. 11

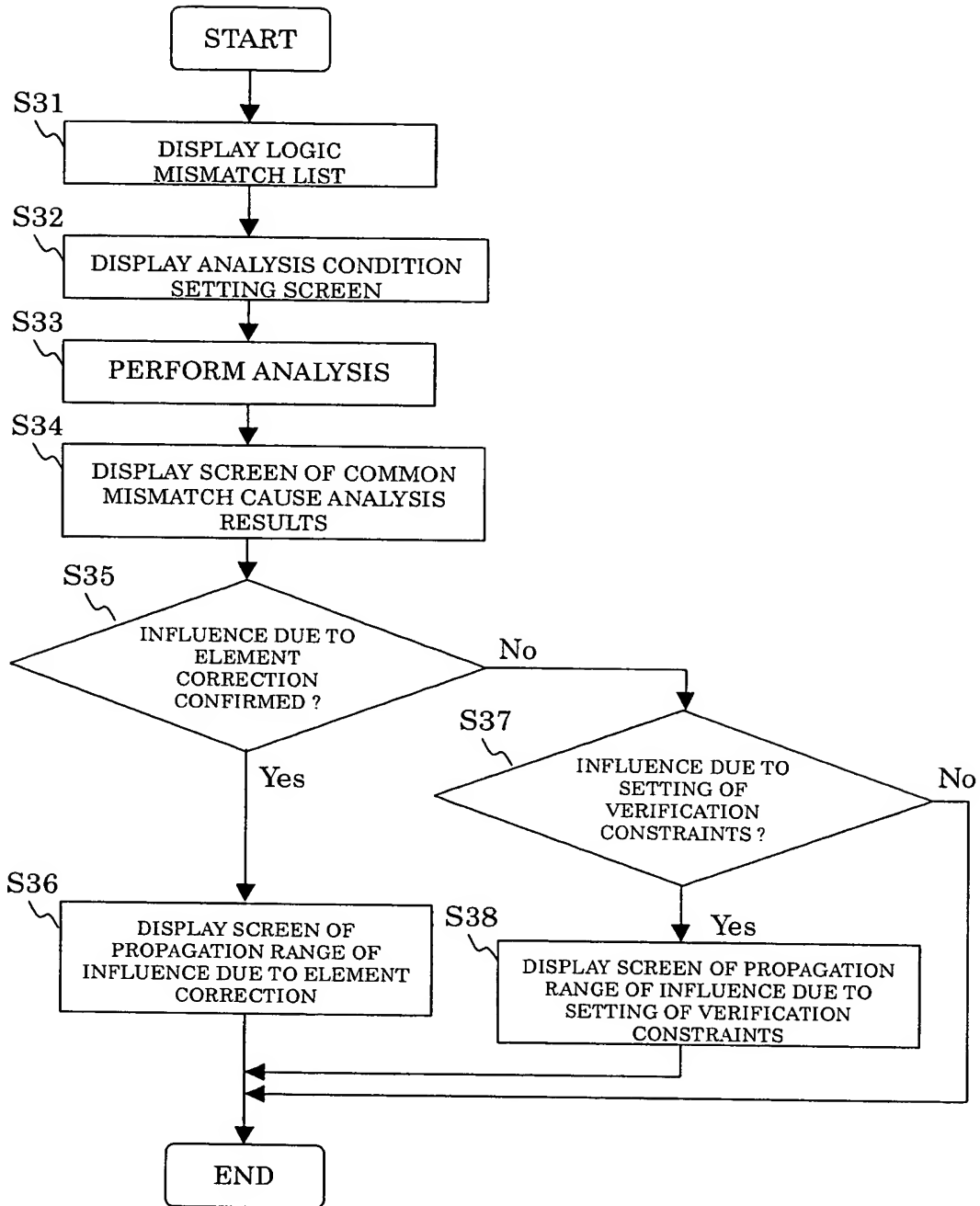


FIG. 12

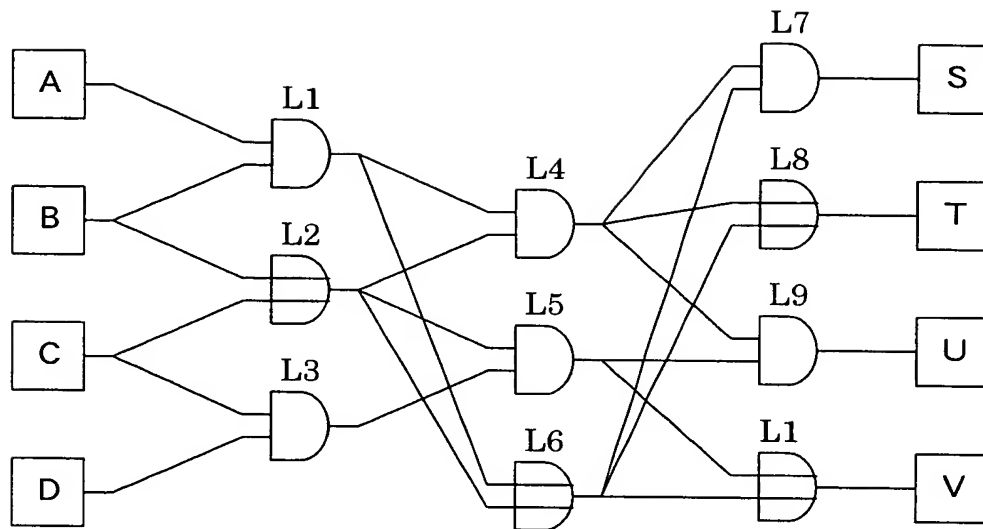


FIG. 13

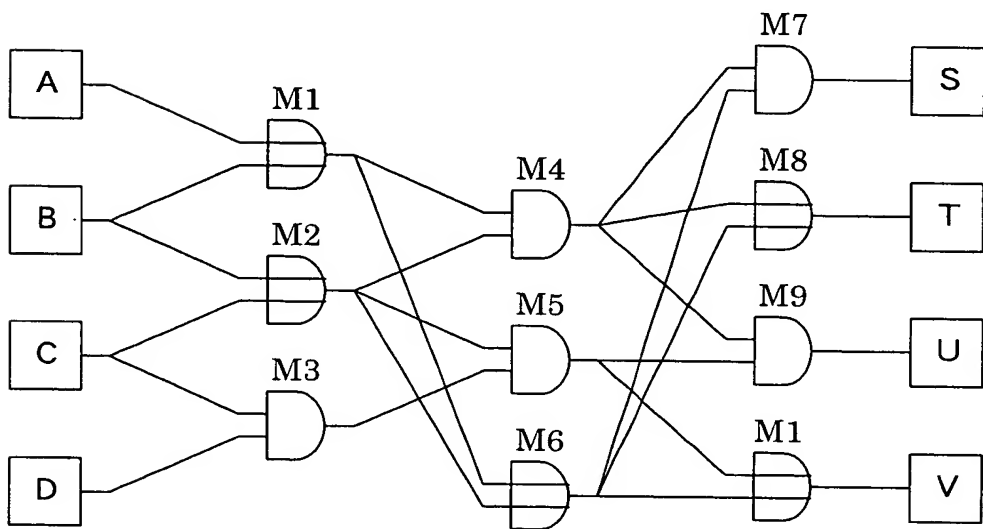


FIG. 14

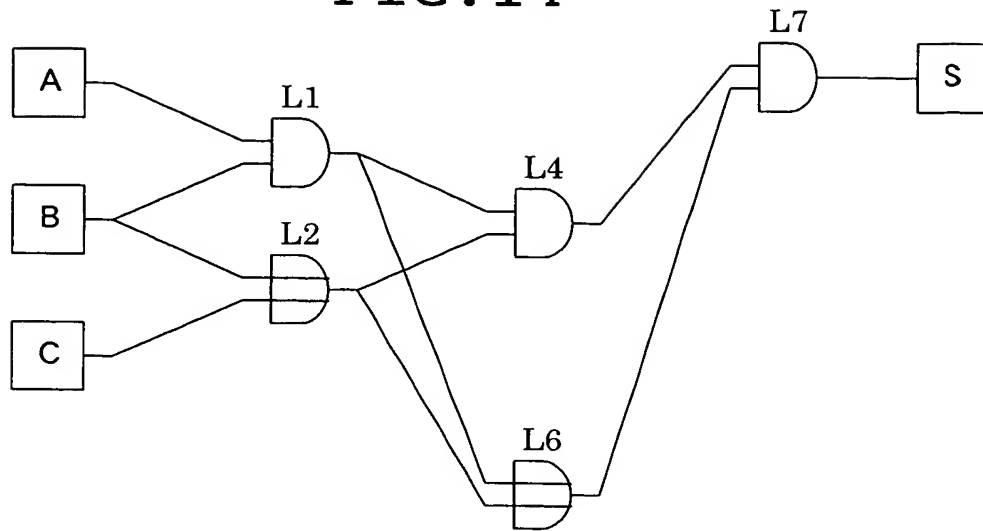


FIG. 15

LOGIC MISMATCH LIST

↑ ↓	1	SPECIFICATION	S	<input checked="" type="checkbox"/>
		IMPLEMENTATION	S	
	2	SPECIFICATION	T	<input checked="" type="checkbox"/>
		IMPLEMENTATION	T	
	3	SPECIFICATION	U	<input checked="" type="checkbox"/>
		IMPLEMENTATION	U	
	4	SPECIFICATION	V	<input checked="" type="checkbox"/>
		IMPLEMENTATION	V	
	5	SPECIFICATION		<input type="checkbox"/>
		IMPLEMENTATION		
	6	SPECIFICATION		<input type="checkbox"/>
		IMPLEMENTATION		

ANALYSIS CONDITION SETTING

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FIG. 16

ANALYSIS CONDITION SETTING					
ANALYSIS ELEMENT KINDS					
AND	<input checked="" type="checkbox"/> ON	<input type="checkbox"/> OFF	ADDER	<input type="checkbox"/> ON	<input checked="" type="checkbox"/> OFF
OR	<input checked="" type="checkbox"/> ON	<input type="checkbox"/> OFF	3STATE	<input type="checkbox"/> ON	<input checked="" type="checkbox"/> OFF
EOR	<input type="checkbox"/> ON	<input checked="" type="checkbox"/> OFF	WIRED LOGIC	<input type="checkbox"/> ON	<input checked="" type="checkbox"/> OFF
NAND	<input type="checkbox"/> ON	<input checked="" type="checkbox"/> OFF	INVERTER	<input type="checkbox"/> ON	<input checked="" type="checkbox"/> OFF
NOR	<input type="checkbox"/> ON	<input checked="" type="checkbox"/> OFF	BUFFER	<input type="checkbox"/> ON	<input checked="" type="checkbox"/> OFF
ENOR	<input type="checkbox"/> ON	<input checked="" type="checkbox"/> OFF			
AND - OR COMBINATION	<input type="checkbox"/> ON	<input checked="" type="checkbox"/> OFF			
SELECTOR	<input type="checkbox"/> ON	<input checked="" type="checkbox"/> OFF			
ANALYSIS ELEMENT CONNECTION STATUS					
MINIMUM INPUT NUMBER	<div>2</div>				
MAXIMUM INPUT NUMBER	<div>NO LIMIT</div>				
MINIMUM OUTPUT BRANCH NUMBER	<div>NO LIMIT</div>				
MAXIMUM OUTPUT BRANCH NUMBER	<div>NO LIMIT</div>				
NUMBER OF OCCURRENCES					
EQUAL TO OR MORE THAN	<div>1</div>				
					72
					<div>ANALYSIS EXECUTION</div>

FIG. 17

COMMON MISMATCH CAUSE ANALYSIS RESULTS							
←→							
SPECIFICATIONS	S	T	U	V			APPLICABLE NUMBER
↑	L 1	■	■	■	■		4
	L 2	■	■	■	■		4
	L 3			■	■		2
	L 4	■	■	■			3
	L 5			■	■		2
	L 6	■	■		■		3
	L 7	■					1
	L 8		■				1
	L 9			■			1
↓	L 1 0				■		1
←→							
IMPLEMENTATION	S	T	U	V			APPLICABLE NUMBER
↑	M 1	■	■	■	■		4
	M 2	■	■	■	■		4
	M 3			■	■		2
	M 4	■	■	■			3
	M 5			■	■		2
	M 6	■	■		■		3
	M 7	■					1
	M 8		■				1
	M 9			■			1
↓	M 1 0				■		1

FIG. 18

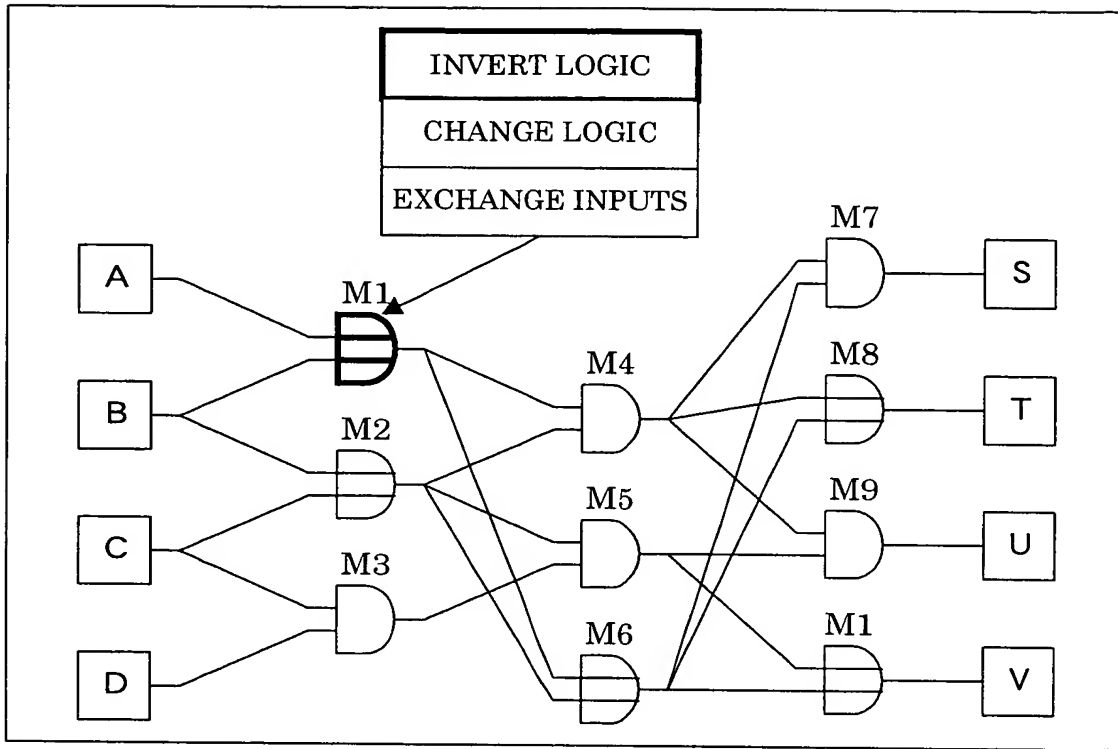


FIG. 19

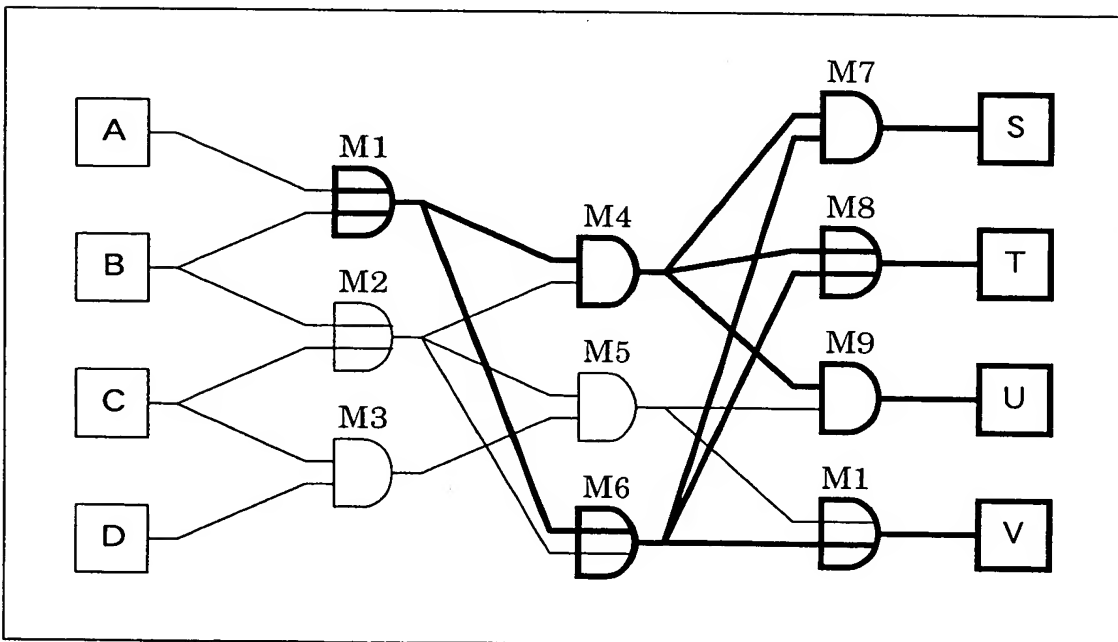


FIG. 20

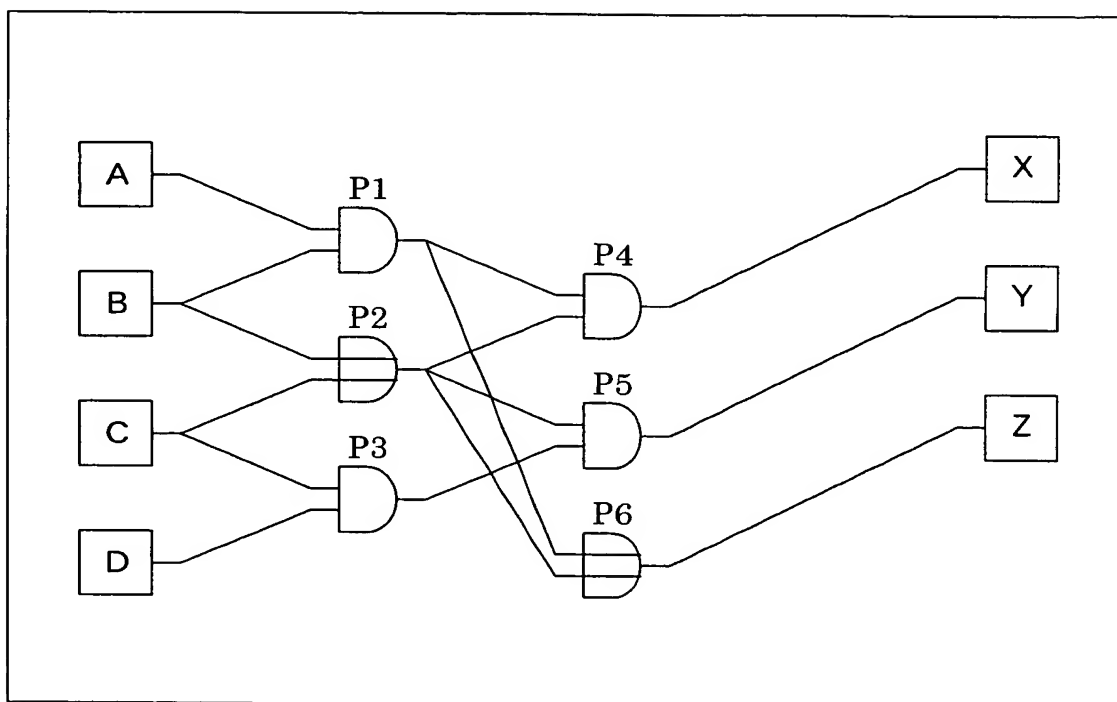


FIG. 21

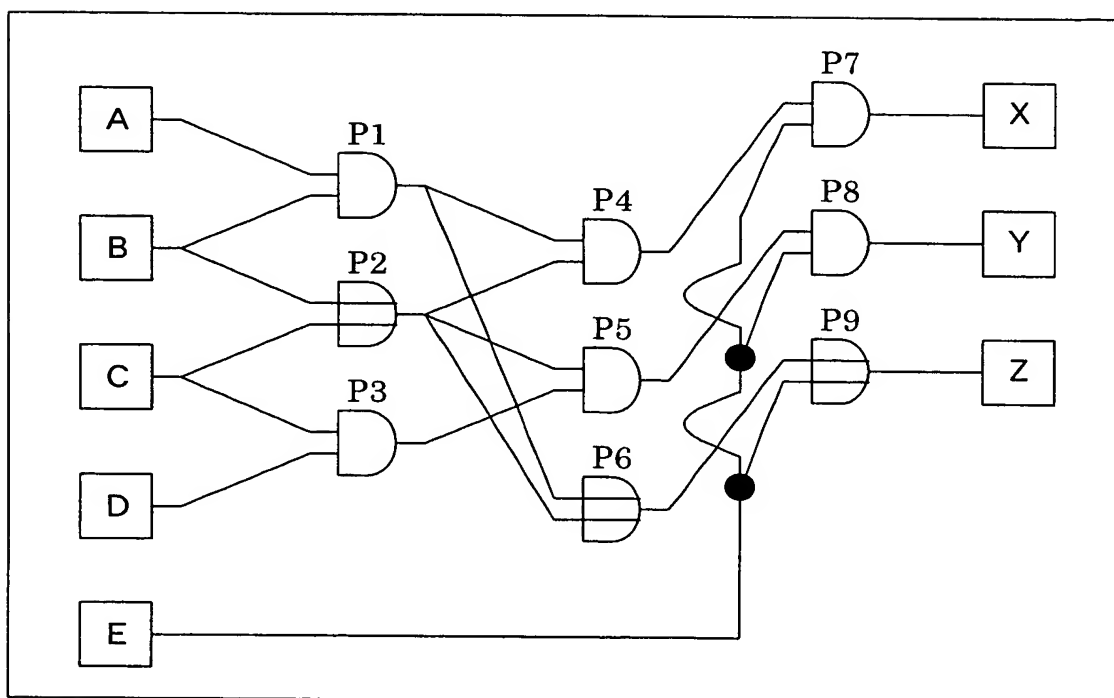


FIG. 22

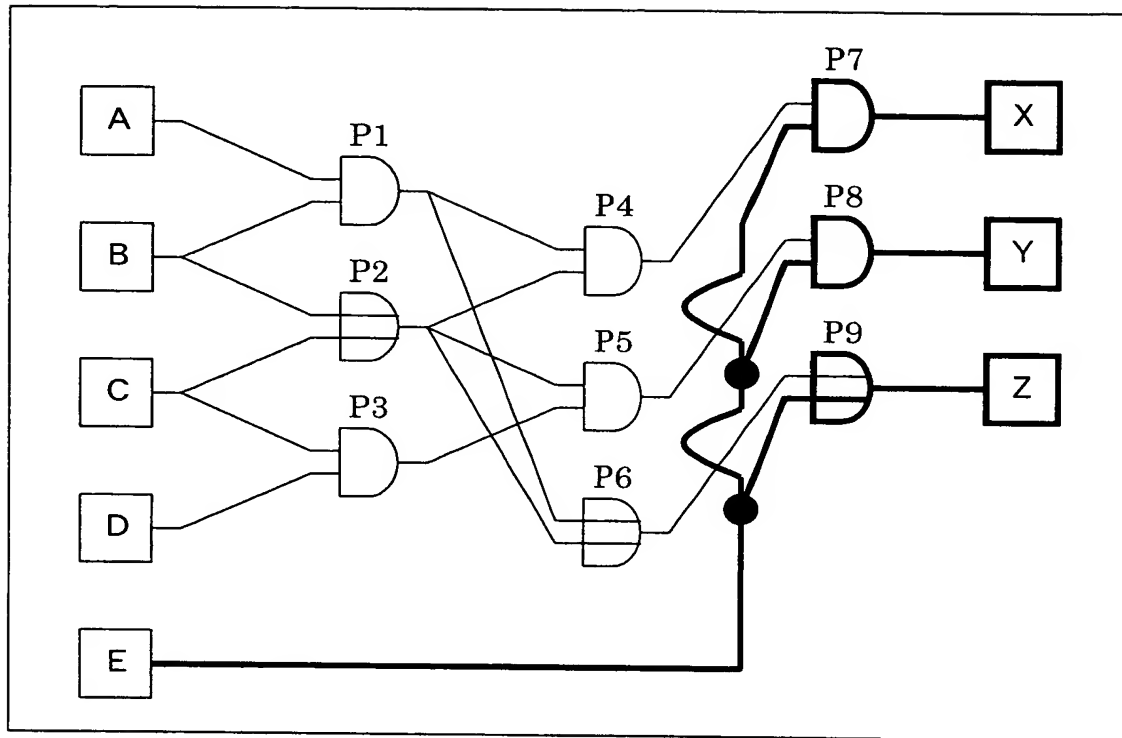


FIG. 23

